REMARKS

Claim Rejections

Claims 2, 6 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Peterson et al. (4,882,454). Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peterson et al. (4,882,454) in view of Nakatani et al. (6,108,903). Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peterson et al. in view of Cutting et al. (5,638,597). Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peterson et al. In view of Kiyota et al. (5,263,248).

Arguments

Claims 2-13 are pending. It is believed that the pending claims specifically set forth each element of Applicant's invention in full compliance with 35 U.S.C. § 112, and define subject matter that is patentably distinguishable over the cited prior art, taken individually or in combination. Namely, the Examiner has not shown that the cited art teaches or suggests using a resin build-up process to form inner layers and a lamination process to form outer layers together on the same PCB. As a result, Applicant submits that the Examiner has not provided a *prima facie* case of obviousness.

Applicant's claims are directed toward: a method of forming a multi-layer printed circuit board (PCB), said multi-layer PCB including one or more cores, a plurality of circuit layers formed by using a resin build-up process or a lamination process to increase the number thereof, said method comprising: forming with said ***resin build-up process*** a resin layer as a first dielectric layer (e.g., 4 in Fig. 2 and 15 in Fig. 3) of ***inner circuit layers*** (e.g., 1a, 1b, 3a, 3b, 5a, and 5b in Fig. 2 and 12a, 12b, 13a, 13b, 14a, 14b, and 15) of said multi-layer PCB; forming on said resin layer a circuit layer as one inner circuit layer for refinement of circuits thereon; and forming a second dielectric layer (e.g., 6 in Fig. 2; 16 and 16a in Fig. 3) as an ***outer circuit layer*** (e.g., 7a, 7b, 6 in Fig. 2 and 11a, 11b in Fig. 3) ***formed with said lamination process*** to enhance a thermal resistance, a copper peel strength, a stiffness, and a thermal stress reliability of said outer circuit layer.

That is, the main characteristic and the primary function of the invention is that said circuit layers located at inner and outer layers of said multi-layer PCB are specifically limited to be formed with said resin build-up process and said lamination process, respectively.

The Examiner has stated, on p.2 of the outstanding Office Action, that Peterson et al. teaches the "sequential build-up of layers (col. 3, lines 61-62)....(101 and 105 formed close to 102)" as well as a "second dielectric layer (col. 3, lines 22-25)." In response, Applicant notes that col. 3, lines 22-25 teaches that the core 102 may be laminated. It is important to note that the core 102 is clearly shown in Figs. 1 and 5 as being a ***middle layer***. As a result, core 102 cannot be said to teach forming an ***outer dielectric layer*** by lamination. Instead, Peterson et al. only disclose that the dielectric layer and the circuit layer of a multi-layer PCB may be formed from different dielectric material and with different process such as is mentioned in col. 3 lines 22-25. Alternatively, the core may instead be laminated with a layer that consists of both the dielectric layer material and conductive foil. Therefore Peterson et al. does not teach that a second or a third layer of a multi-layer PCB is especially limited to be formed from a resin material as a dielectric and with said resin build-up process, and the outer layer of said multi-layer PCB is especially limited to be formed from a laminating dielectric. It follows from the above that the Examiner has not yet presented a *prima facie* case of anticipation with regard to Applicant's claims. As a result, Applicant has traversed the Examiner's rejections under 35 U.S.C. § 102.

Peterson does not teach: a method of forming a multi-layer printed circuit board (PCB), said multi-layer PCB including one or more cores, a plurality of circuit layers formed by using a resin build-up process or a lamination process to increase the number thereof, said method comprising: forming with said resin build-up process a resin layer as a first dielectric layer of said inner circuit layers of said multi-layer PCB; forming on said resin layer a circuit layer as one of said inner circuit layer for refinement of circuits thereon; and forming a second dielectric layer as an outer circuit layer formed with said lamination process to enhance a thermal resistance, a copper peel strength, a stiffness, and a thermal stress reliability of said outer circuit layer.

It is axiomatic in U.S. patent law that, in order for a reference to anticipate a claimed structure, it must clearly disclose each and every feature of the claimed structure. Applicant submits that it is abundantly clear, as discussed above, that Peterson et al. do not disclose each and every feature of Applicant's claims and, therefore, could not possibly anticipate these claims under 35 U.S.C. § 102. Absent a specific showing of these features, Peterson et al. cannot be said to anticipate any of Applicant's claims under 35 U.S.C. § 102.

In order to further explain the invention, Applicant notes that in the 8-layer PCB 100 of Fig. 1, the circuit layers 7a and 7b are the outer circuit layers that form a first layer of the PCB 100, while the circuit layers 1a and 1b, 3a and 3b, and 5a and 5b are the inner circuit layers. The inner circuit layers 5a and 5b and the inner circuit layers 3a and 3b form a second and a third layer, respectively, of the PCB 100, and are also referred to as the second and the third inner circuit layer, respectively. Depending on the above-mentioned steps of the invention, the present invention is characterized in that the resin build-up process and the lamination process are employed to form the inner circuit layers and the outer circuit layers, respectively, of the 8-layer PCB 100. More specifically, the inner circuit layers, such as the second inner circuit layers 5a and 5b, which require refinement of circuits are formed by using a resin material, such as epoxy, as the dielectric to form the resin layers 4 with the resin build-up process through liquid epoxy coating or dry film type epoxy laminating, and then forming the inner circuit layers 5a and 5b. Thereafter, the dielectric layers 6 using the prepreg or the aramid fiber material as the dielectric and the outer circuit layers 7a, 7b are formed with the lamination process. By using the resin build-up process and the lamination process to form different layers on the same one multi-layer PCB, the completed multi-layer PCB 100 is able to include advantages obtainable from the two processes. For example, the second inner circuit layers 5a and 5b of the multi-layer PCB 100 is formed with the resin build-up process offering upgraded circuit refinement to satisfy the circuit design requirement of the multi-layer PCB, and the outer circuit layers 7a and 7b of the multi-layer PCB 100 formed with the lamination process have improved thermal resistance, copper peel strength, stiffness, thermal stress reliability, and size stability. Therefore, the fully completed 8-layer PCB 100 has a quality reliability superior to that of a

multi-layer PCB formed with only one of the conventional forming processes. Therefore, it is the distinguishing features between the invention and the cited prior art of Peterson et al.

However, Peterson et al. do not disclose or teach that an inner layer of a multi-layer PCB is specifically limited to be formed from a resin material as a dielectric and with said resin build-up process, and the outer layer of said multi-layer PCB is especially limited to be formed from a laminating dielectric with said lamination process, as recited by Applicant.

Nakatani et al.is cited as teaching a liquid epoxy, Cutting et al. is cited as teaching dry film type epoxy, and Kiyota et al. is cited as teaching a resin impregnated fiberglass fabric. Applicant does not necessarily acquiesce to these characterizations and further notes that, in any event, the Examiner has not shown that Nakatani et al., Cutting et al., or Kiyota et al. provide the deficiencies of the primary reference. Namely, none of the cited art teaches or suggests using a resin build-up process to form inner layers and a lamination process to form outer layers together on the same PCB.

Even if the teachings of Peterson et al., Nakatani et al., Cutting et al., and Kiyota et al. were combined, as suggested by the Examiner, the resultant combination does not suggest: a method of forming a multi-layer printed circuit board (PCB), said multi-layer PCB including one or more cores, a plurality of circuit layers formed by using a resin build-up process or a lamination process to increase the number thereof, said method comprising: forming with said resin build-up process a resin layer as a first dielectric layer of said inner circuit layers of said multi-layer PCB; forming on said resin layer a circuit layer as one of said inner circuit layer for refinement of circuits thereon; and forming a second dielectric layer as an outer circuit layer formed with said lamination process to enhance a thermal resistance, a copper peel strength, a stiffness, and a thermal stress reliability of said outer circuit layer.

It is a basic principle of U.S. patent law that it is improper to arbitrarily pick and choose prior art patents and combine selected portions of the selected patents on the basis of Applicant's disclosure to create a hypothetical combination which allegedly renders a claim obvious, unless there is some direction in the selected

prior art patents to combine the selected teachings in a manner so as to negate the patentability of the claimed subject matter. This principle was enunciated over 40 years ago by the Court of Customs and Patent Appeals in In re Rothermel and Waddell, 125 USPQ 328 (CCPA 1960) wherein the court stated, at page 331:

> The examiner and the board in rejecting the appealed claims did so by what appears to us to be a piecemeal reconstruction of the prior art patents in the light of appellants' disclosure. ... It is easy now to attribute to this prior art the knowledge which was first made available by appellants and then to assume that it would have been obvious to one having the ordinary skill in the art to make these suggested reconstructions. While such a reconstruction of the art may be an alluring way to rationalize a rejection of the claims, it is not the type of rejection which the statute authorizes.

The same conclusion was later reached by the Court of Appeals for the Federal Circuit in Orthopedic Equipment Company Inc. v. United States, 217 USPQ 193 (Fed.Cir. 1983). In that decision, the court stated, at page 199:

> As has been previously explained, the available art shows each of the elements of the claims in suit. Armed with this information, would it then be non-obvious to this person of ordinary skill in the art to coordinate these elements in the same manner as the claims in suit? The difficulty which attaches to all honest attempts to answer this question can be attributed to the strong temptation to rely on hindsight while undertaking this evaluation. It is wrong to use the patent in suit as a guide through the maze of prior art references, combining the right references in the right way so as to achieve the result of the claims in suit. Monday morning quarterbacking is quite improper when resolving the question of non-obviousness in a court of law.

In In re Geiger, 2 USPQ2d, 1276 (Fed.Cir. 1987) the court stated, at page 1278:

> We agree with appellant that the PTO has failed to establish a *prima facie* case of obviousness. Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching suggestion or incentive supporting the combination.

Applicant submits that there is not the slightest suggestion in either Peterson et al., Nakatani et al., Cutting et al., or Kiyota et al. that their respective teachings may be combined as suggested by the Examiner. Case law is clear that, absent any such teaching or suggestion in the prior art, such a combination cannot be made under 35 U.S.C. § 103.

Neither Peterson et al., Nakatani et al., Cutting et al., nor Kiyota et al. disclose, or suggest a modification of their specifically disclosed structures that would lead one having ordinary skill in the art to arrive at Applicant's claimed structure. Applicant hereby respectfully submits that no combination of the cited prior art renders obvious Applicant's claims.

Summary

In view of the foregoing amendments and remarks, Applicant submits that this application is now in condition for allowance and such action is respectfully requested. Should any points remain in issue, which the Examiner feels could best be resolved by either a personal or a telephone interview, it is urged that Applicant's local attorney be contacted at the exchange listed below.

Respectfully submitted,

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